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Terms	Documents
(bus$3 or (sub adj1 bus$3)) same ((data adj1 flow adj1 processor$1) or (programmable adj1 gate adj1 array$1)) same cell$1	67

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(bus$3 or (sub adj1 bus$3)) same ((data
adj1 flow adj1 processor$1) or
(programmable adj1 gate adj1 array$1))
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USPT	(bus$3 or (sub adj1 bus$3)) same ((data adj1 flow adj1 processor$1) or (programmable adj1 gate adj1 array$1)) same cell$1	67	L5
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USPT	(bus$3 or (sub adj1 bus$3)) same ((data flow processor$1) or (programmable gate array$1)) same cell$1	7847	L3
USPT	(bus$3 or (sub adj1 bus$3)) same ((data flow processor$1) or (programmable gate array$1))	97169	L2
USPT	(bus$3 or (sub adj1 bus$3)) same ((data flow processor$1) or (programmable gate array$1)) same (programmble adj1 cell$1)	0	L1

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(bus$3 or (sub adj1 bus$3)) same ((data adj1 flow adj1 processor$1) or (programmable adj1 gate adj1 array$1)) same cell$1	1

Database: JPO Abstracts Database

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(bus$3 or (sub adj1 bus$3)) same ((data
adj1 flow adj1 processor$1) or
(programmable adj1 gate adj1 array$1))
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Search History

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JPAB	(bus$3 or (sub adj1 bus$3)) same ((data adj1 flow adj1 processor$1) or (programmable adj1 gate adj1 array$1)) same cell$1	1	L6
USPT	(bus$3 or (sub adj1 bus$3)) same ((data adj1 flow adj1 processor$1) or (programmable adj1 gate adj1 array$1)) same cell$1	67	L5
USPT	(bus$3 or (sub adj1 bus$3)) same ((data flow processor$1) or (programmable gate array$1)) same (programmable cell$1)	17619	L4
USPT	(bus$3 or (sub adj1 bus$3)) same ((data flow processor$1) or (programmable gate array$1)) same cell$1	7847	L3
USPT	(bus$3 or (sub adj1 bus$3)) same ((data flow processor$1) or (programmable gate array$1))	97169	L2
USPT	(bus$3 or (sub adj1 bus$3)) same ((data flow processor$1) or (programmable gate array$1)) same (programmble adj1 cell$1)	0	L1

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Terms	Documents
(bus$3 or (sub adj1 bus$3)) same ((data adj1 flow adj1 processor$1) or (programmable adj1 gate adj1 array$1)) same cell$1	1

Database: EPO Abstracts Database

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(bus$3 or (sub adj1 bus$3)) same ((data
adj1 flow adj1 processor$1) or
(programmable adj1 gate adj1 array$1))
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Search History

DB Name	Query	Hit Count	Set Name
EPAB	(bus$3 or (sub adj1 bus$3)) same ((data adj1 flow adj1 processor$1) or (programmable adj1 gate adj1 array$1)) same cell$1	1	L7
JPAB	(bus$3 or (sub adj1 bus$3)) same ((data adj1 flow adj1 processor$1) or (programmable adj1 gate adj1 array$1)) same cell$1	1	L6
USPT	(bus$3 or (sub adj1 bus$3)) same ((data adj1 flow adj1 processor$1) or (programmable adj1 gate adj1 array$1)) same cell$1	67	L5
USPT	(bus$3 or (sub adj1 bus$3)) same ((data flow processor$1) or (programmable gate array$1)) same (programmable cell$1)	17619	L4
USPT	(bus$3 or (sub adj1 bus$3)) same ((data flow processor$1) or (programmable gate array$1)) same cell$1	7847	L3
USPT	(bus$3 or (sub adj1 bus$3)) same ((data flow processor$1) or (programmable gate array$1))	97169	L2
USPT	(bus$3 or (sub adj1 bus$3)) same ((data flow processor$1) or (programmable gate array$1)) same (programmble adj1 cell$1)	0	L1

Document Number 1

Entry 1 of 1 File: EPAB Jun 30, 1998

DOCUMENT-IDENTIFIER: US 5773994 A
TITLE: Method and apparatus for implementing an internal tri-state bus within a programmable logic circuit

FPAR:
An internal tri-state bus is provided in a field programmable gate array (FPGA). The FPGA is comprised of an input/output interface which receives input data and generates output data. User-configurable logic cells are included within the FPGA and are coupled to the input/output interface through interconnect elements. The interconnect elements provide a number of conductive elements which supply input signals to the logic cells and receive output signals generated by the logic cells. At least one of the logic cells contains at least one output and multiple logic elements which typically include AND gates, multiplexers and registers. The logic elements receive input signals from the interconnect elements, perform digital functions on the input signals and generate output signals to the interconnect elements. At least one logic cell in the FPGA contains a tri-state buffer which is coupled to at least one output of the logic cell. In response to an enable signal provided to the tri-state buffer, the tri-state buffer selectively provides one of the output signals to the interconnect elements. The enable signal may be any input signal supplied to a logic cell. Additionally, the enable signal may enable a tri-state buffer to provide an output signal to an interconnect element when the enable signal comprises either a high logic level or a low logic level. In an alternative embodiment an enable signal may be generated by a logic element within the logic cell.

Document Number 1

Entry 1 of 1 File: JPAB Jul 11, 1997

DOCUMENT-IDENTIFIER: JP 09178822 A
TITLE: TESTABLE PROGRAMMABLE GATE ARRAY AND ITS TEST METHOD

FPAR:
SOLUTION: A field programmable gate array(FPGA) 10 has a static RAM (SRAM) 14, a constituting program bit 20, and logic circuits 16, 18. The SRAM 14 holds a constitution data for selectively exciting the constituting states of various programmable resources. The program bit 20 excites various programmable resources of the FPGA 10 according to the constitution data of the related memory cell of the SRAM 14. The circuits 16, 18 access to the SRAM 14, or the circuit 18 receives the data from an address bus 32 and a data bus 34, and provides an address for designating the address of the memory map of the SRAM 14.

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Document Number 1

Entry 1 of 6 File: USPT Feb 15, 2000

US-PAT-NO: 6026227
DOCUMENT-IDENTIFIER: US 6026227 A

TITLE: FPGA logic cell internal structure including pair of look-up tables

DATE-ISSUED: February 15, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Furtek; Frederick C.	Menlo Park	CA	N/A	N/A
Mason; Martin T.	San Jose	CA	N/A	N/A
Luking; Robert B.	Catonsville	MD	N/A	N/A

US-CL-CURRENT: 716/16

ABSTRACT:

A field programmable gate array has a matrix of programmable logic cells and a bus network of local and express bus lines. The bus network effectively partitions the matrix into blocks of cells with each block having its own distinct set of local bus lines. Express bus lines extend across more than one block of cells by means of repeater switch units that also connect local bus lines to express bus lines. The grouping of cells into blocks with repeaters aligned in rows and columns at the borders between blocks creates spaces at the corners of blocks that can be filled with RAM blocks, other memory structures, specialized logic structures or other dedicated function elements that are connected to the bus network. The RAM blocks can be single or dual port SRAM addressed through the bus lines. Pairs of adjacent columns of RAM blocks may be commonly addressed by the same set of bus lines. Other specialized or dedicated logic might also fill those corner spaces. Logic cells are directly connected to neighboring cells, including diagonally adjacent cells, and are also connected to local bus lines. The arrangement of express bus lines is preferably staggered in such a way that they connect to non-consecutive repeaters in an alternating manner. I/O pads connect to cells at the perimeter of the matrix and to the bus network. Preferably, pads are connectable to more than one cell and more than one row or column of bus lines, and each perimeter cell can be connected to any of several I/O pads.
19 Claims, 21 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 20

Document Number 2

Entry 2 of 6 File: USPT Jan 11, 2000

US-PAT-NO: 6014509
DOCUMENT-IDENTIFIER: US 6014509 A

TITLE: Field programmable gate array having access to orthogonal and diagonal adjacent neighboring cells

DATE-ISSUED: January 11, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Furtek; Frederick C.	Menlo Park	CA	N/A	N/A
Mason; Martin T.	San Jose	CA	N/A	N/A
Luking; Robert B.	Catonsville	MD	N/A	N/A

US-CL-CURRENT: 716/16; 716/17

ABSTRACT:

A field programmable gate array (FPGA) comprising a matrix of programmable logic cells, a bus network of local and express bus lines, and a system of perimeter I/O pads is disclosed. Logic cells are directly connected to neighboring nearest cells, including diagonally and orthogonally adjacent cells, and are also connected to local bus lines. Such direct cell-to-cell connections allow both directions of signal propagation. I/O pads connect to cells at the perimeter of the matrix and to the bus network. Preferably, I/O pads are connectable to more than one cell and more than one row or column of bus lines, and each perimeter cell can be connected to any of several I/O pads.
18 Claims, 21 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 20

Document Number 1

Entry 1 of 1 File: USPT Aug 24, 1999

US-PAT-NO: 5943242
DOCUMENT-IDENTIFIER: US 5943242 A

TITLE: Dynamically reconfigurable data processing system

DATE-ISSUED: August 24, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Vorbach; Martin Andreas	Karlsruhe	N/A	N/A	DEX
Munch; Robert Markus	Karlsruhe	N/A	N/A	DEX

US-CL-CURRENT: 716/17; 712/11, 712/14, 712/18

ABSTRACT:

A data processing system, wherein a data flow processor (DFP) integrated circuit chip is provided which comprises a plurality of orthogonally arranged homogeneously structured cells, each cell having a plurality of logically same and structurally identically arranged modules. The cells are combined and facultatively grouped using lines and columns and connected to the input/output ports of the DFP. A compiler programs and configures the cells, each by itself and facultatively grouped, such that random logic functions and/or linkages among the cells can be realized. The manipulation of the DFP configuration is performed during DFP operation such that modification of function parts (MACROs) of the DFP can take place without requiring other function parts to be deactivated or being impaired.
23 Claims, 30 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 13

Document Number 1

Entry 1 of 1 File: USPT Aug 24, 1999

US-PAT-NO: 5943242
DOCUMENT-IDENTIFIER: US 5943242 A

TITLE: Dynamically reconfigurable data processing system

DATE-ISSUED: August 24, 1999

INT-CL: [6] G06F 13/00, G06F 17/00

US-CL-ISSUED: 364/491; 395/800.11, 395/800.14, 395/800.18

US-CL-CURRENT: 716/17; 712/11, 712/14, 712/18

FIELD-OF-SEARCH: 364/488-491, 364/749, 364/745, 364/716.02, 364/716.03, 364/716.01, 364/716.05, 395/800, 395/707, 395/800.16, 395/800.14, 395/800.15, 395/800.18, 395/800.11

Document Number 1

Entry 1 of 1 File: USPT Aug 24, 1999

DOCUMENT-IDENTIFIER: US 5943242 A
TITLE: Dynamically reconfigurable data processing system

BSPR:
This objective is accomplished by providing an integrated circuit (chip) with a plurality of cells which, in particular, are arranged orthogonally to one another, each with a plurality of logically same and structurally identically arranged cells, whose arrangement and internal bus structure is extremely homogeneous so as to facilitate programming. Nonetheless, it is conceivable to accommodate within a data flow processor cells with different cell logics and cell structures in order to increase the capacity in that, for example, there exist for memory access other cells than for arithmetic operations. A certain specialization can be advantageous, especially for neuronal networks. Coordinated with the cells is a loading logic by way of which the cells, by themselves and facultatively grouped in so-called MACROs, are so programmed that, for one, selective logical functions but, for another, also the linking of cells among themselves can be realized widely. This is achieved in that for each individual cell a certain memory location is available in which the configuration data are filed. These data are used to switch multiplexers or transistors in the cell so as to guarantee the respective cell function (refer to FIG. 12).

DEPR:
According to the first exemplary embodiment illustrated in FIG. 9, a plurality of integrated circuits 20--analogous to the arrangement of the cells--are arranged in the orthogonal raster, with adjoining circuits being coupled, or linked, to one another via local bus lines 21. Consisting for instance of 16 integrated circuits 20, the computer structure features input/output lines I/O, by way of which the computer quasi communicates, i.e., transacts with the outside world. The computer according to FIG. 9 also features a memory 22, which according to the illustrated exemplary embodiment consists of two separate memories, each composed of RAM, ROM as well as a dual-ported RAM wired as shared memory to the compiler, which memories can be realized likewise as write-read memories or also as read memories only. Hierarchically coordinated with, or superimposed upon, the computer structure described so far is the compiler 30, by means of which the integrated circuits (data flow processor) 20 can be programmed and configured and linked.

Document Number 1

Entry 1 of 1 File: USPT

US-PAT-NO: 5113498
DOCUMENT-IDENTIFIER: US 5113498 A

TITLE: Input/output section for an intelligent cell which provides sensing, bidirectional communications and control

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Evan; Shabtai	Saratoga	CA	N/A	N/A
Sander; Wendell B.	Los Gatos	CA	N/A	N/A

US-CL-CURRENT: 710/8; 364/221, 364/221.1, 364/228, 364/228.1, 364/231.8, 364/232.2, 364/232.8, 364/237.8, 364/238.3, 364/240, 364/240.8, 364/240.9, 364/241.9, 364/242.94, 364/242.96, 364/244, 364/244.3, 364/244.6, 364/244.9, 364/247, 364/247.2, 364/247.5, 364/247.6, 364/247.7, 364/247.8, 364/254, 364/254.5, 364/259, 364/259.1, 364/259.3, 364/259.5, 364/260, 364/260.3, 364/260.4, 364/260.81, 364/262, 364/262.3, 364/262.4, 364/262.9, 364/270, 364/271, 364/271.4, 364/271.5, 364/281.3, 364/284, 364/284.3, 364/284.4, 364/DIG1

ABSTRACT:

A network for providing sensing, communications and control is described. A plurality of intelligent cells each of which comprises an integrated circuit having a processor and input/output section are coupled to the network. Each of the programmable cells receives when manufactured a unique identification number (48 bits) which remains permanently within the cell. The cells can be coupled to different media such as power lines, twisted, pair, radio frequency, infrared ultrasonic, optical coaxial, etc., to form a network. The preferred embodiment of the cell includes a multiprocessor and multiple I/O subsections where any of the processors can communicate with any of the I/O subsections. This permits the continual execution of a program without potential interruptions caused by interfacing with the I/O section. The I/O section includes programmable A-to-D and programmable D-to-A converters as well as other circuits for other modes of operation.
21 Claims, 30 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 18

Document Number 1

Entry 1 of 1 File: USPT

US-PAT-NO: 5113498
DOCUMENT-IDENTIFIER: US 5113498 A

TITLE: Input/output section for an intelligent cell which provides sensing, bidirectional communications and control

INT-CL: [5] G06F 15/16, G06F 3/00

US-CL-ISSUED: 395/275; 364/DIG.1, 364/221.1, 364/221, 364/238.3, 364/228.1, 364/237.2 , 364/259.3, 364/259, 395/200

US-CL-CURRENT: 710/8; 364/221, 364/221.1, 364/228, 364/228.1, 364/231.8, 364/232.2, 364/232.8, 364/237.8, 364/238.3, 364/240, 364/240.8, 364/240.9, 364/241.9, 364/242.94, 364/242.96, 364/244, 364/244.3, 364/244.6, 364/244.9, 364/247, 364/247.2, 364/247.5, 364/247.6, 364/247.7, 364/247.8, 364/254, 364/254.5, 364/259, 364/259.1, 364/259.3, 364/259.5, 364/260, 364/260.3, 364/260.4, 364/260.81, 364/262, 364/262.3, 364/262.4, 364/262.9, 364/270, 364/271, 364/271.4, 364/271.5, 364/281.3, 364/284, 364/284.3, 364/284.4, 364/DIG1

FIELD-OF-SEARCH: 364/2MS, 364/9MS